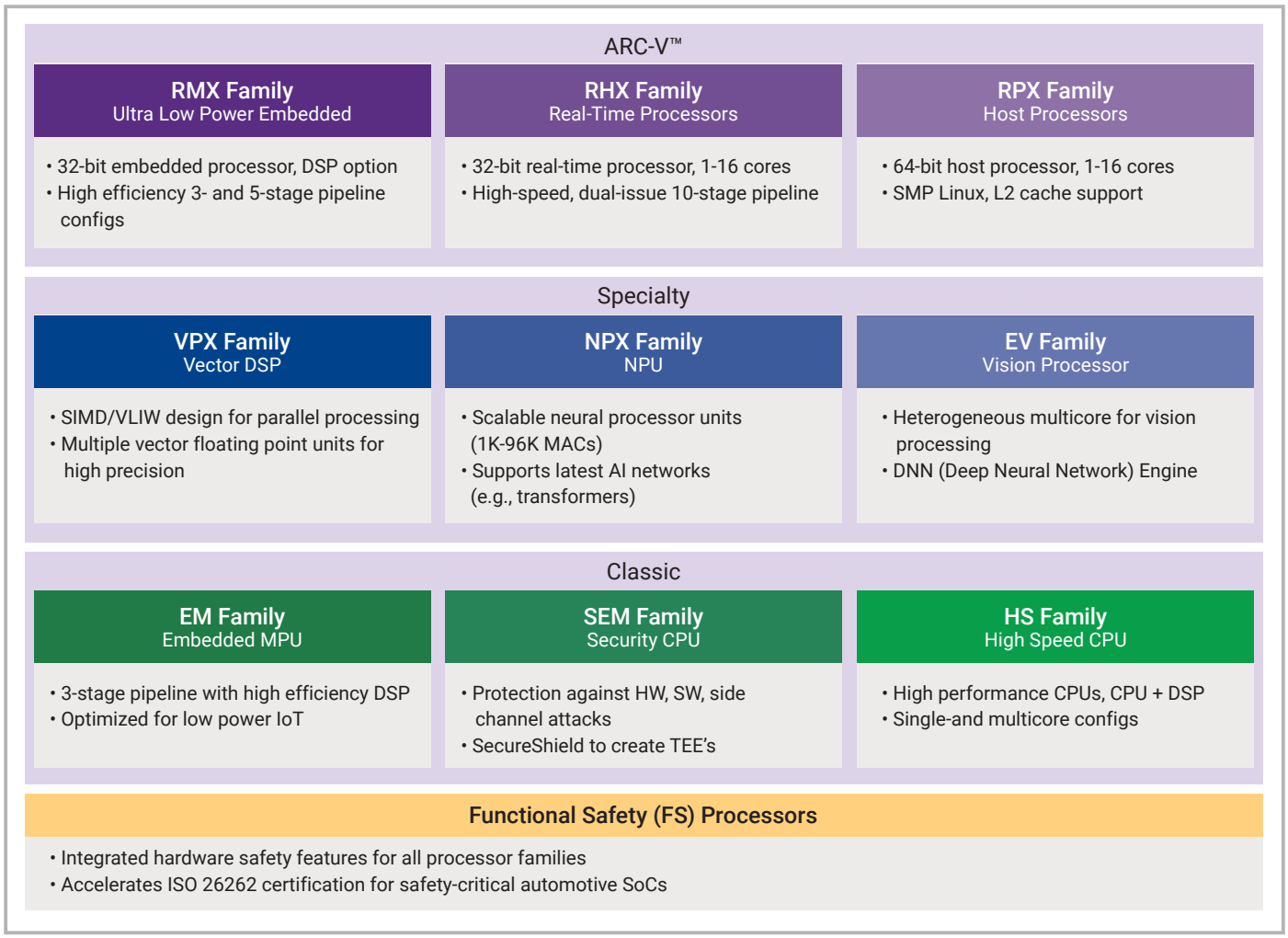
SYNOPSYS®

# Synopsys Processor Solutions

- Scalable family of RISC-V based processors, wide-vector processors, neural processors, vision processors, and subsystems
- Maximum power and area efficiency (DMIPS/mW, DMIPS/$mm^2$) for embedded applications
- Highly configurable so each instance can be optimized
- Extensible instruction set enables application-specific customizations
- Integrated tool suite with broad hardware and software ecosystem support

## Synopsys Processor IP Portfolio




## Processor IP Solutions

Synopsys' processor IP solutions are based on a portfolio of processors, subsystems, software, development systems and tools. ARC-V processor IP is based on the open standard RISC-V instruction set architecture (ISA) and ARC processors are based on a flexible and proven 32-/64-bit ISA with features optimized for a broad range of embedded applications:

- Performance-efficient designs deliver maximum performance while consuming a minimum amount of power and silicon area
- Highly configurable processors can be performance-and power-optimized for each instance on an SoC while sharing a common programming model
- Extensible ISAs support user-defined custom instructions, enabling integration of users' proprietary hardware to accelerate application-specific tasks
- Streamlined system integration through the ability to closely couple memories and directly map peripherals to the core, reducing system latency and cost

## ARC-V Processor IP

The Synopsys ARC-V processors leverage the proven microarchitecture of the existing ARC processor offerings, while giving customers access to the expanding RISC-V ecosystem. The Synopsys ARC-V portfolio, based on the RISC-V ISA, includes high-performance, mid-range, and ultra-low power families, as well as functional safety (FS) versions, to address a broad range of application workloads.

### ARC-V RMX Processors

The 32-bit ARC-V RMX series includes the 3-stage pipeline RMX-100 and the 5-stage pipeline RMX-500 processors, which are optimized for ultra-low power embedded applications. The processors offer optional DSP support for greater signal processing efficiency. The RMX processors offer ISO 26262 ASIL B and D FuSa compliance as well as ISO 21434 cybersecurity compliance.

### ARC-V RHX Processors

The 32-bit ARC-V RHX-100 series consists of superscalar, single-core and multicore processors optimized for efficient real-time applications. It includes support for coherent accelerators and real-time hardware virtualization as well as optional RVV extensions (RHX-100V/105V). For safety-critical applications, the RHX-100 series offers functional safety compliant versions of all the processors in the series.

### ARC-V RPX Processors

The 64-bit ARC-V RPX-100 series are multicore processors with 64-bit RISC-V defined profile support for both user and supervisor modes. The multicore ARC-V RPX-105 supports SMP Linux and shared L3 cache. It offers configurations up to 16 cores and is optimized for efficient host processing performance for a variety of applications. The RPX-100 series also offers functional safety compliant versions of its processors.

## ARC Specialty Processor IP

Processor IP tuned for best power, performance, and area for dedicated application domains.

### ARC VPX DSP IP

The ARC VPX DSP Family includes the ARC VPX2, VPX3 and VPX5 processors, which are based on an extended ARCv2DSP instruction set architecture and optimized for a broad range of high-performance signal processing applications such as IoT sensor fusion, natural language processing, RADAR/LiDAR, engine control and vision processing. The VPX DSPs implement a configurable, energy-efficient very long instruction word (VLIW) / single instruction-multiple data (SIMD) architecture that combines scalar and vector execution units to enable a high degree of parallel processing. The VPX2 and VPX3 DSPs are available in single- and dual-core configurations and support 128-bit and 256-bit vector word lengths, respectively. VPX5 is available in single-, dual-, and quad-core configurations and supports 512-bit vector word lengths. To speed application software development, the VPX family is supported by Synopsys' ARC MetaWare Development Toolkit, which provides a comprehensive and vector length-agnostic software programming environment that enables code portability among all members of the VPX family. The tool suite includes an optimizing C/ C++ compiler, debugger, instruction set simulator, as well as DSP, machine learning inference, computer vision and math libraries.

### ARC NPX Neural Processing Unit IP

The Synopsys ARC NPX6 NPU IP family provides a high-performance, power- and area-efficient IP solution for a range of applications requiring AI-enabled SoCs. The ARC NPX6 NPU IP is designed for deep learning algorithm coverage including both computer vision tasks such as object detection, image quality improvement, and scene segmentation, and for broader AI applications such as audio and natural language processing.

The architecture is based on individual cores that can scale from 1K MACs to 96K MACs for a single AI engine performance of over 250 TOPS (or over 400 TOPS with sparsity). The NPX6 family integrates control connectivity features that synchronize communication signals and manage power, enabling the implementation of multiple NPU instances that can deliver up to 3,500 TOPS of performance on a single SoC. The NPX6 NPU IP family offers optional 16-bit floating point support inside the neural processing hardware, maximizing layer performance and simplifying the transition from GPUs used for AI prototyping to high-volume power- and area-optimized SoCs.

### Embedded Vision Processors

The ARC EV7x Embedded Vision processors are fully programmable and configurable IP cores that have been optimized for artificial intelligence and deep learning applications, combining the flexibility of software solutions with the low cost and low power consumption of hardware. The EV7x Processors integrate scalar, vector DSP and deep neural network (DNN) processing units for highly accurate and fast vision processing. The ARC EV7x Vision Processors integrate up to four enhanced vector processing units (VPUs) and a DNN accelerator with up to 3,520 MACs.

The EV Processors are designed to integrate seamlessly into an SoC and can be used with any host processors and operate in parallel with the host. With up to four vector DSPs that operate in parallel to the DNN engine, the EV7x Processors provide scalable performance that supports convolutional neural network (CNN) and recurrent neural network (RNN) graphs. In addition, an optional IEEE 754-compliant vector floating point unit, integrated into the vector DSP core, and its supporting software, offer performance levels of up to 328 Gigaflops for single precision operations and 655 Gigaflops for half precision operations. The embedded deep neural network engine accelerates the processing of CNN/RNN executables, enabling accurate and power-efficient object detection, image classification, and convolutional LSTMs.

## ARC Classic Processors

Family of 32-/64-bit processors based on the flexible and proven ARCv2 and ARCv3 instruction sets.

### ARC EM Processors

The ARC EM Family includes the ARCv2 ISA-based ARC EM4 and EM6 as well as the DSP-enhanced EM5D, EM7D, EM9D and EM11D. All ARC EM processors support instruction and data CCMs and the EM6, EM7D and EM11D additionally support instruction and data caches. The EM9D and EM11D feature support for XY memories to deliver higher levels of signal processing efficiency. The ultra-compact EM cores feature excellent code density, small size and very low power consumption, making them ideal for power-critical and area-sensitive embedded and deeply embedded applications.

Along with optional FPU, MPU, µDMA, Real-Time Trace and ARConnect for multicore integration, the EM Family also offers an Enhanced Security Package , which provides tamper protection features and enables designers to create a trusted execution environment that protects their systems and software from evolving security threats.

In addition, the CryptoPack option for EM cores uses ARC Processor EXtension (APEX) technology to accelerate common cryptographic software algorithms.

### ARC SEM Security Processors

The Synopsys ARC SEM Family includes the ARCv2 ISA-based ARC SEM110 and SEM120D security processors to protect against logical, hardware and physical attacks. The SEM processors include a secure MPU that enables the creation of a Trusted Execution Environment (TEE) to protect secure functions from software vulnerabilities. The ARC SEM110 is a 32-bit RISC core that is optimized for performance, power, and area efficiency. The ARC SEM120D has an added DSP instruction set and unified multiply/ MAC unit. The ARC CryptoPack, FPU and µDMA licensable options are available for the ARC SEM processors.

The ASIL D compliant ARC SEM130FS Safe and Secure Processor simplifies development of safety-critical automotive applications while enabling designers to integrate security into their SoC to protect against logical, hardware and physical attacks. The ARC SEM130FS processor is supported by a comprehensive set of safety work products and the ARC MetaWare Toolkit for Safety with ASIL D Ready certified compiler to generate ISO 26262 compliant code.

### ARC HS Processors

The ARC HS Family includes the 32-bit ARC HS56, HS57D, HS58, HS58 and 64-bit HS66 processors, which are based on the ARCv3 instruction set architecture (ISA), and the ARCv2 ISA based HS34, HS36, HS38, HS44, HS46, HS48, HS45D and HS47D processors.

All HS processors support closely coupled memories (CCMs), which enable single-cycle access to instructions and data. The HS family processors (except HS34, HS44 and HS45D) add up to 64 KB each of instruction and data caches. The HS38, HS48 and HS58 also include an advanced memory management unit (MMU) to support embedded Linux and other high-end operating systems.

The HS45D, HS47D, and HS57D support more than 150 DSP-optimized instructions, delivering a unique combination of high-performance control and high-efficiency digital signal processing. HS processors are optimized for GHz+ operating speeds with minimum area and power consumption, making them ideally suited for embedded applications with very high-performance requirements. The HS3x and HS4x processors are available in single-core, dual-core, and quad-core configurations, and the HS5x and HS6x are available in single-core and multicore configurations with support for up to 12 cores.

### ARC Processor EXtension (APEX) Technology

ARC processors support the addition of user-defined extensions to the core. These extensions can take the form of more processor and auxiliary registers, new instructions, and/or additional condition code tests. Custom instructions enable designers to efficiently add their proprietary hardware to the processor to further increase application performance. ARC-V processors are aligned with custom extensions defined within the RISC-V standard.

### ARC Functional Safety Processors

The Synopsys ARC functional safety (FS) processors support ASIL B and ASIL D safety levels to simplify safety-critical automotive SoC development and accelerate ISO 26262 qualification. The portfolio includes the ARC EM22FS, SEM130FS, HS4xFS, EV7xFS, VPXxFS, NPX6FS and ARC-V safety processors with integrated hardware safety features such as redundant processors, error-correcting code (ECC), parity protection, safety monitors, and user-programmable windowed watchdog timers to detect system errors. The Synopsys MetaWare Development Toolkit for Safety (EM22FS, HS4xFS, SEM130FS, VPXxFS and ARC-V safety processors) MetaWare EV Development Toolkit for Safety (EV7xFS), and MetaWare MX Development Toolkit for Safety (NPX6FS) help software developers accelerate the development of ISO 26262-compliant code.

## ARC Processor Subsystems

### ARC IoT Communications IP Subsystem

The Synopsys ARC IoT Communications IP Subsystem is an integrated, pre-verified software-defined modem integrating an ARC EM11D processor, tightly coupled memories, Viterbi accelerator, dedicated peripherals and software libraries to deliver efficient real-time control and DSP performance for IoT applications requiring low bandwidth wireless communication.

### ARC Data Fusion IP Subsystem

The Synopsys ARC Data Fusion IP Subsystem is a complete, pre-verified, hardware and software solution that includes the choice of an energy-efficient ARC EM5D, EM7D, EM9D or EM11D processor for both RISC and DSP processing, accompanied by a collection of I/O functions and fast math (trigonometric) accelerators. The included software libraries contain small-footprint drivers for all I/O, DSP functions and optional audio processing software library supporting gain control, mixer and sample rate conversion. The integrated solution is optimized for “always on” data fusion combining sensor, voice, gesture and audio processing typically implemented
in IoT edge devices.

### ARC Sensor and Control IP Subsystem

The Synopsys ARC Sensor and Control IP Subsystem is optimized to process data from digital and analog sensors, offloading the host processor and enabling more power-efficient processing of sensor and control data. The fully configurable IP subsystem includes the choice of an ARC EM4 or EM6 processor, serial digital interfaces, data converter interfaces and hardware accelerators.

| ARC Subsystems | Supported Processors | Hardware Accelerators | Integrated Peripherals | Included Software |
|---|---|---|---|---|
| ARC IoT Communications IP Subsystem | EM11D | ✓ | SPI, UART(s), GPIO, Digital Front End (DFE), PMU and RTC | DSP library, base communications library, device drivers |
| ARC Data Fusion IP Subsystem | EM5D, EM7D, EM9D, EM11D | ✓ | SPI, I2C, I3C, PWM, UART, PDM, ADC I/F, DAC I/F, APB I/F, GPIO | DSP library, audio processing library, peripheral I/O drivers (bare metal), reference designs ARC Sensor & Control |
| ARC Sensor and Control IP Subsystem | EM4, EM6 | ✓ | SPI, I2C, PWM, UART, ADC I/F, DAC I/F, APB I/F, GPIO | DSP library, peripheral I/O drivers (bare metal) |

Table 1: Synopsys ARC Processor Subsystems

## Software Development Support

### Software Tool Chains

To accelerate the SoC development cycle, Synopsys' processor IP is supported by a complete and integrated development tool suite, including tools for configuration, software development and simulation. This enables users to efficiently build, debug, profile and optimize their embedded software apllications.

The MetaWare Development Toolkit contains all the components needed to support the development, debugging and optimization of embedded applications for ARC and ARC-V processors. The compiler and debugger are fully integrated in a modern, developer-friendly IDE and the Toolkit also comes with the nSIM Instruction-Set Simulator.

In addition, Synopsys' ARC EM and HS processors are supported by the latest open-source GNU Tool Chain, including the GNU GCC Compiler, GDB Debugger, libraries and utilities.

The ARC EV Vision Processor family is supported by MetaWare EV Development Toolkit, a comprehensive, high-productivity software development environment based on common embedded vision standards, including OpenVX and OpenCL C. The tool suite enables the development of efficient computer vision applications on the EV processor's vector engine as well as automatic mapping and optimization of neural networks graphs on the dedicated DNN accelerator. The mapping tools support Caffe and Tensorflow frameworks, as well as the ONNX neural network interchange format. For maximum flexibility and future-proofing, the tool can also distribute computations between the VPU and DNN resources to support new and emerging neural networks.

The NPX Neural Processor family is supported by the ARC MetaWare MX Development Toolkit, complete set of tools including the MetaWare NN SDK and the MetaWare Virtual Platforms SDK. The MetaWare NN SDK is a MetaWare MX component for AI/ML developers and users which supports a broad range of open-source frameworks. It includes a neural network compiler to automatically reduce computation, memory, and bandwidth requirements and a NN inference engine with a simple interface to deploy NN models on ARC processors.

### Simulators

Synopsys offers a variety of simulation products spanning automatically-generated, cycle-accurate simulators to fast, functional instruction-set simulators (ISS). Synopsys' simulation products enable software development prior to silicon being available.

The Synopsys ARC nSIM Pro Simulator is primarily used for software development and debugging. It can operate as a very fast ISS, it includes a Near Cycle Accurate Mode (NCAM), and also supports the Synopsys Virtualizer prototyping tools.

Synopsys ARC xCAM is a 100% cycle-accurate simulator that is primarily used for hardware verification, but can also be used to do final optimizations of critical software routines. The xCAM model is automatically generated from the processor configuration and can be used to evaluate different hardware scenarios.

### Operating Systems

To support applications that require fast, real-time response, Synopsys offers MQX RTOS. MQX occupies a very small memory footprint and supports fast context switch times.

ARC processor cores are supported by open-source operating systems available from official project repositories. Synopsys enhances and maintains the Linux kernel and the Zephyr RTOS to run optimally on ARC processor cores.

### Third-party Ecosystem

The ARC Access Program expands the choice of embedded software and hardware solutions available for ARC and ARC-V processor IP. This program builds on the ecosystem of third parties supporting the ARC and RISC-V architectures with software development tools, real-time operating systems (RTOSes), middleware and stacks, semiconductor IP and design services.

The ARC Access Program helps customers to:

- Develop ARC-based embedded solutions faster by leveraging compatible products from leading embedded industry vendors
- Reduce project risk by taking advantage of design solutions pre-ported and tested for ARC processor IP
- Save on development costs and resources by using products optimized for ARC-based designs

## ARC EM Software Development Platform

The ARC EM Software Development Platform accelerates software development and debug of ARC EM processor-based system-on-chips (SoCs) for a wide range of ultra-low power embedded applications such as IoT, sensor fusion, and voice applications. The ARC EM Software Development Platform includes a configurable hardware board with commonly used peripherals including motion sensors, flash memory, Bluetooth, and Wi-Fi and is extensible with Arduino, mikroBUS and Pmod connectors. Downloadable platform packages with hardware and software configuration information are available, providing a flexible software development platform.

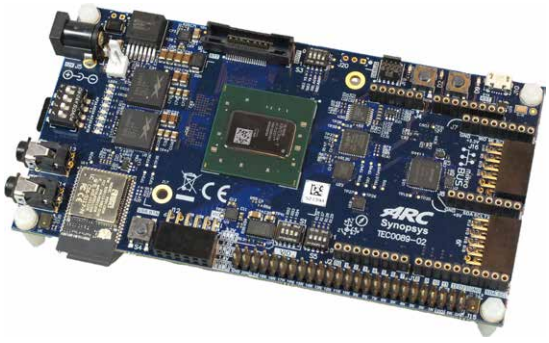


Figure 1: ARC EM Software Development Platform

### ARC HS Development Kits

The ARC HS Development Kits are ready-to-use software development platforms that include a multicore ARC HS3x-based or ARC HS4xD-based chip, implemented in a TSMC 28HPM process, that integrates a wide range of interfaces including Ethernet, USB, SDIO, I2C, SPI, UART, and GPIO, as well as a GPU. The kit also features an on-board WiFi and Bluetooth module. This combination of ARC HS processors and the comprehensive set of peripherals allow developers to build and debug complex software on a fully-featured hardware platform. Software support includes ARC Linux and the embARC Open Software platform available from the embARC.org web portal.

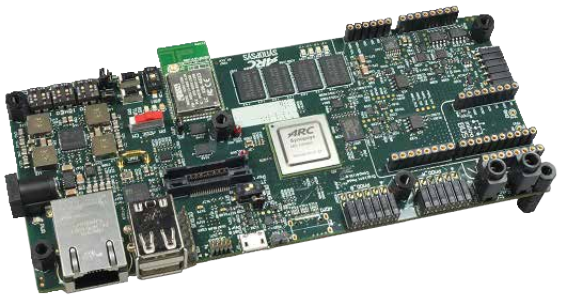


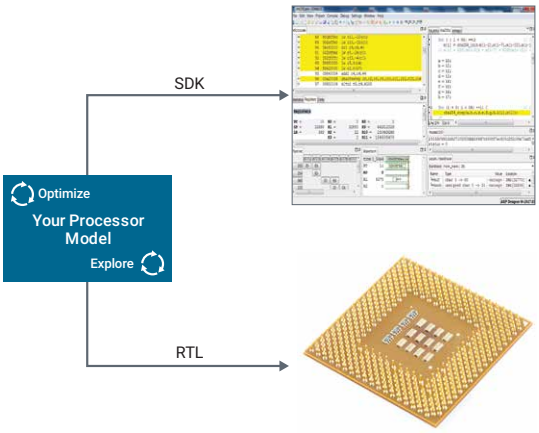
Figure 2: ARC HS Development Kit

## ASIP Designer

Modern multicore SoCs often include specialized processing functions that sometimes cannot be addressed efficiently with off-the-shelf processor IP. These custom processing elements are often manually designed in fixed-function RTL, requiring significant engineering effort and lacking post-silicon programmability. Application-specific instruction-set processors (ASIPs) close this gap.

ASIPs are software-programmable hardware (e.g., custom processors, DSPs or programmable accelerators) tailored to a specific application or class of algorithms. They are ideally suited for specialized DSP applications, enabling designers to take advantage of inherent instruction- and data-level parallelism and customized instruction and datapath elements to achieve high levels of performance in a minimal power envelope. Because they are programmable, ASIPs also give design teams the flexibility to support post-silicon modifications as well as specifications that are still evolving.

ASIP Designer is a tool suite to accelerate the design, programming and verification of ASIPs that brings ASIP design within easy reach of every SoC team. Using a single processor description language, ASIP Designer automatically generates both a software development kit (SDK) including a C/C++ compiler, both cycle-accurate and instruction-accurate simulators, and a fully featured debugger, as well as synthesizable RTL. This allows for efficient exploration of architectural choices and a rapid path to silicon implementation.



# Synopsys Processor Families

| ARC-V RMX Series - Ultra-low Power 32-bit RISC-V Processors for Embedded Applications | | | | | | |
|---|---|---|---|---|---|---|
| **Key Features*** | **RMX-100** | **RMX-100D** | **RMX-110-FS** | **RMX-500** | **RMX-500D** | **RMX-510-FS** |
| 3-stage pipeline based on RISC-V ISA | ✓ | ✓ | ✓ | | | |
| 5-stage pipeline based on RISC-V ISA | | | | ✓ | ✓ | ✓ |
| Instruction and data closely coupled memory (CCMs) | Up to 2MB | Up to 2MB | Up to 2MB | Up to 2MB | Up to 2MB | Up to 2MB |
| L1 instruction cache | Up to 64KB | Up to 64KB | Up to 64KB | Up to 64KB | Up to 64KB | Up to 64KB |
| L1 data cache | | | | Up to 64KB | Up to 64KB | Up to 64KB |
| Physical Memory Protection (PMP) (RISC-V MPU) | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Enhanced sleep modes | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Fixed/vector DSP processing support | | ✓ | ✓ | | ✓ | ✓ |
| 32x32 MUL/MAC unit | | ✓ | ✓ | | ✓ | ✓ |
| Programmable watchdog timer | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Power management interface / DVFS support | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| ECC on memories | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| IS026262 Functional Safety Compliance | | | ✓ | | | ✓ |
| ISO21434 Cybersecurity Compliance | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Arm AMBA AXI, AHB & AHB-Lite interfaces | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| FPU (single, double-precision, IEEE 754-2008 compliant) | Opt | Opt | Opt | Opt | Opt | Opt |
| Real-time Trace (ARC Trace I/F) | Opt | Opt | Opt | Opt | Opt | Opt |
| **Example Applications** | | | | | | |
| Motor control, smart metering, sensors, keyless entry, body electronics, safety management, AIoT, wearables, hearables, consumer SSD, eMMC/SD cards, LPWAN, M2M, BLE control | | | | | | |

*Subject to change

Opt = separately licensable options

# Synopsys Processor Families (Continued)

| ARC-V RHX Series - Power-Efficient 32-bit RISC-V Processors for Real-time Applications | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Key Features*** | **RHX-100** | **RHX-105** | **RHX-100V** | **RHX-105V** | **RHX-110-FS** | **RHX-115-FS** | **RHX-110V-FS** | **RHX-115V-FS** |
| 10-stage, dual-issue pipeline based on RISC-V ISA | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Instruction and data closely coupled memory (CCMs) | Up to 16MB | Up to 16MB | Up to 16MB | Up to 16MB | Up to 16MB | Up to 16MB | Up to 16MB | Up to 16MB |
| L1 instruction & data cache | Up to 128KB | Up to 128KB | Up to 128KB | Up to 128KB | Up to 128KB | Up to 128KB | Up to 128KB | Up to 128KB |
| Cluster shared memory / shared L2 cache | Up to 16MB | Up to 16MB | Up to 16MB | Up to 16MB | Up to 16MB | Up to 16MB | Up to 16MB | Up to 16MB |
| Multi-core support up to 16 CPUs | | ✓ | | ✓ | | ✓ | | ✓ |
| Real-time hardware virtualization | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Physical Memory Protection (PMP) (RISC-V MPU) | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Enhanced sleep modes & architectural clock gating | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| RVV (RISC-V) vector extension support | | | ✓ | ✓ | | | ✓ | ✓ |
| L1 cache coherency | | ✓ | | ✓ | | ✓ | | ✓ |
| Power management interface / DVFS support | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| ECC on memories | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| IS026262 Functional Safety Compliance | | | | | ✓ | ✓ | ✓ | ✓ |
| ISO21434 Cybersecurity Compliance | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Arm AMBA AXI, AHB interfaces | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Floating point (half, single, double-precision, IEEE 754-2008 compliant) | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Cluster DMA | Opt | Opt | Opt | Opt | Opt | Opt | Opt | Opt |
| Sv32 Memory Management Unit (RISC-V MMU) | Opt | Opt | Opt | Opt | Opt | Opt | Opt | Opt |
| Real-time Trace (ARC Trace I/F) | Opt | Opt | Opt | Opt | Opt | Opt | Opt | Opt |
| **Example Applications** | | | | | | | | |
| Robotics, medical devices, factory automation, domain controller, infotainment, display controller, laser printing, enterprise SSD, computational storage, NAS, NIC, ethernet switches, home networking, WAP | | | | | | | | |

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# Synopsys Processor Families (Continued)

| ARC-V RPX Series - Performance-Efficient 64-bit RISC-V Host Processors | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Key Features*** | **RPX-100** | **RPX-105** | **RPX-100V** | **RPX-105V** | **RPX-110-FS** | **RPX-115-FS** | **RPX-110V-FS** | **RPX-115V-FS** |
| 10-stage, dual-issue pipeline based on RISC-V ISA | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| L1 instruction & data cache | Up to 64KB | Up to 64KB | Up to 64KB | Up to 64KB | Up to 64KB | Up to 64KB | Up to 64KB | Up to 64KB |
| L2 cache (unified) | Up to 128KB | Up to 128KB | Up to 128KB | Up to 128KB | Up to 128KB | Up to 128KB | Up to 128KB | Up to 128KB |
| Cluster shared memory / shared L3 cache | Up to 16MB | Up to 16MB | Up to 16MB | Up to 16MB | Up to 16MB | Up to 16MB | Up to 16MB | Up to 16MB |
| Multi-core support up to 16 CPUs | | ✓ | | ✓ | | ✓ | | ✓ |
| Hardware virtualization | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Sv32 Memory Management Unit (RISC-V MMU) | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Enhanced sleep modes & architectural clock gating | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| RVV (RISC-V) vector extension support | | | ✓ | ✓ | | | ✓ | ✓ |
| L1 / L2 cache coherency | | ✓ | | ✓ | | ✓ | | ✓ |
| Power management interface / DVFS support | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| ECC on memories | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| IS026262 Functional Safety Compliance | | | | | ✓ | ✓ | ✓ | ✓ |
| ISO21434 Cybersecurity Compliance | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Arm AMBA CHI, ACE-Lite interfaces | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Floating point (half, single, double-precision, IEEE 754-2008 compliant) | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Cluster DMA | Opt | Opt | Opt | Opt | Opt | Opt | Opt | Opt |
| Real-time Trace (ARC Trace I/F) | Opt | Opt | Opt | Opt | Opt | Opt | Opt | Opt |
| **Example Applications** | | | | | | | | |
| Avionics, medical imaging, factory automation, zonal controller, powertrain, V2I/V2X/V2V, baseband control, VR/AR, storage area networks (SAN), routers, cellular basestation | | | | | | | | |

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# Synopsys Processor Families (Continued)

| ARC VPX Family—High-Performance DSP for Signal Processing Applications | | | | | | |
|---|---|---|---|---|---|---|
| Key Features | VPX2 | VPX3 | VPX5 | VPX2FS | VPX3FS | VPX5FS |
| Vector-length (bit) | 128 | 256 | 512 | 128 | 256 | 512 |
| Scalar execution unit | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Three vector execution units | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Dual SIMD multiply units (8-, 16- and 32-bit) | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Linear algebra/math vector floating point engine | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Vector data closely coupled memory (VCCM) | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Arm® AMBA® AXI™ and AHB-Lite™ interfaces | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Single-, and dual-core configurations | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Quad-core configurations | | | ✓ | | | ✓ |
| Enhanced sleep modes and architectural clock gating | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| L1 and I/O cache coherency unit | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| ECC on memories | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Safety certified | | | | ✓ | ✓ | ✓ |
| Power management interface/DVFS support | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Scalar FPU (single- and double-precision, IEEE754-2008 compliant) | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Memory Protection Unit (MPU) | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| 3D DMA engine | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Dual floating point vector engines (half and single precision) | Opt | Opt | Opt | Opt | Opt | Opt |
| L2 cache | Opt | Opt | Opt | Opt | Opt | Opt |
| Real-Time Trace (RTT) | Opt | Opt | Opt | Opt | Opt | Opt |
| Example Applications | | | | | | |
| Automotive driver assist systems (ADAS), RADAR, LiDAR, powertrain, engine control, multi-sensor fusion, baseband comunications, industrial automation, smart home, IoT, and voice/speech/natural language processing | | | | | | |

Opt = separately licensable options

| ARC NPX6 NPU Family–AI/Neural Processing | | | | | | | |
|---|---|---|---|---|---|---|---|
| | NPX6 1K | NPX6 4K | NPX6 8K | NPX6 16K | NPX6 32K | NPX6 64K | NPX6 96K |
| MACs | 1,024 | 4,096 | 8,192 | 16,384 | 32,768 | 65,536 | 98,304 |
| DMA | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| L2 Shared Memory | 0-64 MB | 0-64 MB | 0-64 MB | 0-64 MB | 0-64 MB | 0-64 MB | 0-64 MB |
| L2 Controller | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Tensor Accelerator | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Tensor Floating Point Unit (FPU) | Opt | Opt | Opt | Opt | Opt | Opt | Opt |
| Trace | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Memory Management Unit (MMU) | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Virtualization | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Functional Safety | | | | | | | |
| Example Applications | | | | | | | |
| Advanced driver assistance systems (ADAS), surveillance, digital TVs and cameras, data center and edge server inference | | | | | | | |

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# Synopsys Processor Families (Continued)

| ARC NPX6FS NPU Family–AI/Neural Processing | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | NPX6FS 1K | NPX6FS 4K | NPX6FS 8K | NPX6FS 16K | NPX6FS 32K | NPX6FS 48K | NPX6FS 64K | NPX6FS 96K |
| MACs | 1,024 | 4,096 | 8,192 | 16,384 | 32,768 | 49,152 | 65,536 | 98,304 |
| DMA | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| L2 Shared Memory | 0-64 MB | 0-64 MB | 0-64 MB | 0-64 MB | 0-64 MB | 0-64 MB | 0-64 MB | 0-64 MB |
| L2 Controller | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Tensor Accelerator | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Tensor Floating Point Unit (FPU) | Opt | Opt | Opt | Opt | Opt | Opt | Opt | Opt |
| Trace | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Memory Management Unit (MMU) | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Virtualization | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Functional Safety | ASIL B/D | ASIL B/D | ASIL B/D | ASIL B/D | ASIL B/D | ASIL B/D | ASIL B/D | ASIL B/D |
| **Example Applications** | | | | | | | | |
| Advanced driver assistance systems (ADAS), surveillance, digital TVs and cameras, data center and edge server inference | | | | | | | | |

Opt = separately licensable options

| EV Family—Fast, Accurate Object Detection for Embedded Vision Applications | | | | | | |
|---|---|---|---|---|---|---|
| **Key Features** | EV71 | EV72 | EV74 | EV71FS | EV72FS | EV74FS |
| # vector processing units | 1 | 2 | 4 | 1 | 2 | 4 |
| Vector engine MACs | 64 | 128 | 256 | 64 | 128 | 256 |
| DMA option | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| L1 cache coherency | | ✓ | ✓ | | ✓ | ✓ |
| DNN/CNN Engine option (MACs) | 880, 1760, or 3520 | 880, 1760, or 3520 | 880, 1760, or 3520 | 880, 1760, or 3520 | 880, 1760, or 3520 | 880, 1760, or 3520 |
| Vector floating point unit option | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Real-time trace (RTT) | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Functional safety | | | | Integrated (ASIL B, C, or D) | Integrated (ASIL B, C, or D) | Integrated (ASIL B, C, or D) |
| **Example applications** | | | | | | |
| Autonomous vehicles, ADAS, surveillance, facial detection/recognition, augmented reality, SLAM | | | | | | |

# Synopsys Processor Families (Continued)

| ARC EM Family—Ultra-Compact, Ultra Low-Power Processors for Deeply Embedded Applications | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Key Features** | **EM4** | **EM6** | **EM5D** | **EM7D** | **EM9D** | **EM11D** | **EM22FS** |
| 3-stage pipeline based on ARCv2 ISA | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Up to 2 MB instruction and data closely coupled memory | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Enhanced sleep modes | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Arm® AMBA® AHB and AHB-Lite™ interfaces | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| 32 KB of instruction and data caches | | ✓ | | ✓ | | ✓ | ✓ |
| DSP enhanced ARCv2DSP ISA with 150+ DSP instructions and 32x32 MUL/MAC | | | ✓ | ✓ | ✓ | ✓ | ✓ |
| Up to 8 registers for fast context switch | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Programmable watchdog timer | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| | | | | | | | |
| 32x32 MUL/MAC unit | | | ✓ | ✓ | ✓ | ✓ | ✓ |
| XY memory | | | | | ✓ | ✓ | |
| Power management interface/DVFS support | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| ECC on memories | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Enhanced Security Package | Opt | | Opt | | | | Opt |
| µDMA controller | Opt | Opt | Opt | Opt | Opt | Opt | Opt |
| CryptoPack (cryptographic software algorithm acceleration) | Opt | Opt | Opt | Opt | Opt | Opt | Opt |
| FPU (single- and double-precision, IEEE754-2008 compliant) | Opt | Opt | Opt | Opt | Opt | Opt | Opt |
| Memory Protection Unit (MPU) | Opt | Opt | Opt | Opt | Opt | Opt | ✓ |
| Real-Time Trace (RTT) | Opt | Opt | Opt | Opt | Opt | Opt | Opt |
| ARConnect (ARC EM multicore connect IP) | Opt | Opt | Opt | Opt | | | |
| **Example Applications** | | | | | | | |
| IoT, wearables, sensor processing and control, smart appliances, always-on sensors, SSDs, flash controllers, automotive safety systems (ISO 26262) | | | | | | | |

Opt = separately licensable options

# Synopsys Processor Families (Continued)

| ARC SEM Family—Security Processors for Low-Power Embedded Applications | | | |
|---|---|---|---|
| **Key Features** | **SEM110** | **SEM120D** | **SEM130FS** |
| 3-stage pipeline based on ARCv2 ISA | ✓ | ✓ | ✓ |
| Up to 2 MB instruction and data closely coupled memory | ✓ | ✓ | ✓ |
| Secure privilege mode orthogonal to kernel/user mode | ✓ | ✓ | ✓ |
| Enhanced secure MPU with context ID for secure or normal operation | ✓ | ✓ | ✓ |
| Up to 16 configurable protected regions and per region scrambling capability | ✓ | ✓ | ✓ |
| Uniform instruction timing | ✓ | ✓ | ✓ |
| Timing/power randomization | ✓ | ✓ | ✓ |
| In-line instruction scrambling | ✓ | ✓ | ✓ |
| Data and instruction path integrity checking | ✓ | ✓ | ✓ |
| Integrated watchdog timer | ✓ | ✓ | ✓ |
| Secure debug capability with user-defined challenge/response mechanism | ✓ | ✓ | ✓ |
| DSP-enhanced ARCv2DSP ISA with 100+ DSP instructions and 32x32 MUL/MAC | | ✓ | ✓ |
| Functional Safety | | | ✓ |
| µDMA controller | Opt | Opt | Opt |
| CryptoPack (cryptographic software algorithm acceleration) | Opt | Opt | Opt |
| FPU (single- and double-precision, IEEE754-2008 compliant) | Opt | Opt | Opt |
| **Example Applications** | | | |
| IoT industrial, smart cities, smart meters, embedded SIM, healthcare, automotive | | | |

Opt = separately licensable options

# Synopsys Processor Families (Continued)

| HS3x and HS4x/D Processors (ARCv2 ISA)—High-Speed 32-bit Processors for High-End Embedded Applications | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Key Features** | **HS34** | **HS36** | **HS38** | **HS44** | **HS46** | **HS48** | **HS45D** | **HS47D** | **HS46FS** | **HS47DFS** | **HS48FS** |
| 10-stage pipeline based on ARCv2 ISA | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Dual-issue pipeline | | | | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Up to 16 MB instruction and data closely coupled memory (CCM) | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| 64-bit loads and stores | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Up to 8 register files for fast context switching | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Arm® AMBA® AXI™ and AHB-Lite™ interfaces | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Single-, dual- and quad-core configurations | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| 64 KB of instruction and data caches | | ✓ | ✓ | | ✓ | ✓ | | ✓ | ✓ | ✓ | ✓ |
| Enhanced sleep modes and architectural clock gating | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| DSP enhanced ARCv2DSP with 150+ DSP instructions | | | | | | | ✓ | ✓ | | ✓ | |
| L1 and I/O cache coherency | | ✓ | ✓ | | ✓ | ✓ | | ✓ | ✓ | ✓ | ✓ |
| 64-bit ARC Processor EXtensions (APEX) | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| ECC on memories | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| 32x32 MUL/MAC unit | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Power management interface/DVFS support | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Memory Management Unit (MMU) supporting 40-bit addressing | | Opt | ✓ | | Opt | ✓ | | Opt | Opt | Opt | ✓ |
| L2 cache | | Opt | ✓ | | Opt | ✓ | | Opt | Opt | Opt | ✓ |
| Enhanced Security Package | Opt | Opt | Opt | Opt | Opt | Opt | Opt | Opt | Opt | Opt | Opt |
| FPU (single- and double-precision, IEEE754-2008 compliant) | Opt | Opt | Opt | Opt | Opt | Opt | Opt | Opt | Opt | Opt | Opt |
| Memory Protection Unit (MPU) | Opt | Opt | | Opt | Opt | | Opt | Opt | Opt | Opt | Opt |
| Cluster DMA | Opt | Opt | Opt | Opt | Opt | Opt | Opt | Opt | Opt | Opt | Opt |
| Real-Time Trace (RTT) | Opt | Opt | Opt | Opt | Opt | Opt | Opt | Opt | Opt | Opt | Opt |
| **Example Applications** | | | | | | | | | | | |
| Solid state drive (SSD) controller, automotive systems, home gateways, baseband control, home networking, edge devices, embedded Linux-based devices | | | | | | | | | | | |

Opt = separately licensable options

## Synopsys Processor Families (Continued)

| ARC HS5x and HS6x Processors (ARCv3 ISA)—High-Speed 32-/64-bit Processors for High-End Embedded Applications | | | | | |
|---|---|---|---|---|---|
| **Key Features** | **HS56** | **HS57D** | **HS58** | **HS66** | **HS68** |
| 10-stage pipeline based on ARCv2 ISA | ✓ | ✓ | ✓ | ✓ | ✓ |
| Dual-issue pipeline | ✓ | ✓ | ✓ | ✓ | ✓ |
| Up to 16 MB instruction and data closely coupled memory (CCM) | ✓ | ✓ | ✓ | ✓ | ✓ |
| 64-bit loads and stores | ✓ | ✓ | ✓ | | |
| 128-bit loads and stores | | | | ✓ | ✓ |
| Up to 8 register files for fast context switching | ✓ | ✓ | ✓ | ✓ | ✓ |
| Arm® AMBA® AXI™ and AHB-Lite™ interfaces | ✓ | ✓ | ✓ | ✓ | ✓ |
| Up to 12-core configurations | ✓ | ✓ | ✓ | ✓ | ✓ |
| 64 KB of instruction and data caches | ✓ | ✓ | ✓ | ✓ | ✓ |
| Enhanced sleep modes and architectural clock gating | ✓ | ✓ | ✓ | ✓ | ✓ |
| DSP enhanced ARCv2DSP with 150+ DSP instructions | | ✓ | | | |
| L1 and I/O cache coherency | ✓ | ✓ | ✓ | ✓ | ✓ |
| 64-bit ARC Processor EXtensions (APEX) | ✓ | ✓ | ✓ | | |
| 128-bit ARC Processor EXtensions (APEX) | | | | ✓ | ✓ |
| ECC on memories | ✓ | ✓ | ✓ | ✓ | ✓ |
| 32x32 MUL/MAC unit | ✓ | ✓ | ✓ | | |
| 2x 32x32 MUL/MAC unit | | | | ✓ | ✓ |
| Power management interface/DVFS support | ✓ | ✓ | ✓ | ✓ | ✓ |
| Memory Management Unit (MMU) supporting 40-bit addressing | | | Opt | | Opt |
| 52-bit physical, 64-bit virtual address space | | | | Opt | Opt |
| L2 cache | Opt | Opt | Opt | Opt | Opt |
| Enhanced Security Package | Opt | Opt | Opt | Opt | Opt |
| FPU (single- and double-precision, IEEE754-2008 compliant) | Opt | Opt | Opt | | |
| 128-bit SIMD FPU IEEE754 compliant | | | | Opt | Opt |
| Memory Protection Unit (MPU) | Opt | Opt | Opt | Opt | Opt |
| Cluster DMA | Opt | Opt | Opt | Opt | Opt |
| Real-Time Trace (RTT) | Opt | Opt | Opt | Opt | Opt |
| **Example Applications** | | | | | |
| Solid state drive control, automotive systems, wireless modems, networking, IoT nodes and gateways | | | | | |

Opt = separately licensable options

## About Synopsys IP

Synopsys is a leading provider of high-quality, silicon-proven semiconductor IP solutions for SoC designs. The broad Synopsys IP portfolio includes logic libraries, embedded memories, analog IP, wired and wireless interface IP, security IP, embedded processors and subsystems. To accelerate IP integration, software development, and silicon bring-up, Synopsys' IP Accelerated initiative provides architecture design expertise, pre-verified and customizable IP subsystems, hardening, and signal/power integrity analysis. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enables designers to reduce integration risk and accelerate time-to-market.

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11/28/23.CS1235112032-Processor-Solutions-brochure.