SYNOPSYS®

DesignWare IP for Automotive SoCs

Overview

Automotive SoC architectures are evolving to support the transition to centralized domain compute modules, complex FinFET processes, artificial intelligence (AI) capabilities, and new Advanced Driver Assistance Systems (ADAS) and vehicle-to-everything (V2X) communication. Synopsys provides the broadest portfolio of automotive-grade DesignWare Interface, Processor, Security and Foundation IP with highest levels of safety, security, quality and reliability. Designers can accelerate their SoC-level design and qualification with: ASIL B and D Ready IP developed and assessed specifically for ISO 26262 random hardware faults, ARC processors compliant for both ASIL D random hardware faults and ASIL D systematic, ISO 9001-certified Quality Management System, IP designed and tested as per AEC-Q100, SoC-Level safety manager, IP for automotive grade 0, 1, and 2 temperature, and IP on 22FDX and FinFET processes including 16-nm and 7-nm with 5-nm in development.

Advanced Driver Assistance Systems

Synopsys' DesignWare Automotive IP is implemented using a Functional Safety (FuSa) compliant development flow for ISO 26262 random hardware and systematic faults for ASIL B and D safety levels. Synopsys' DesignWare IP portfolio for safety-critical automotive SoCs includes functional safety packages, which consist of Failure Modes Effects and Diagnostics Analysis (FMEDA) reports, Safety Manuals, and certification reports to accelerate SoC level safety assessments and help designers reach their target ASILs. Synopsys implements a safety culture, policies, processes, strategies with independent safety managers for FuSa-related IP development. In addition, the DesignWare ARC processors provide SoC level safety manager to monitor, detect and report random failures under normal operation. Synopsys' high-performance, small area, and low-power IP portfolio, available in advanced FinFET processes, helps designers accelerate ISO 26262 assessment and achieve ASIL targets.

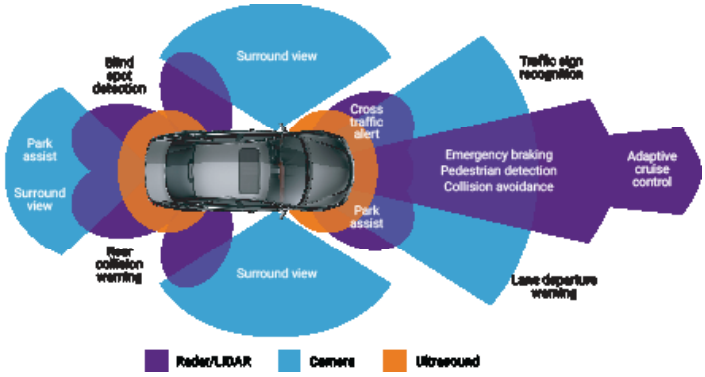

Figure 1: ADAS applications

Benefits of Synopsys DesignWare IP for ADAS

- Industry's widest selection of interface IP, including LPDDR5/4/4X, Ethernet AVB/TSN, PCI Express, CCIX, MIPI, UFS and HDMI, offers high quality and reliability for driver assistance systems
- ARC EV Vision Processors support fast, accurate object detection, classification and scene segmentation by implementing deep neural network (DNNs) with OpenCV and OpenVX software programming environments
- ARC Functional Safety Processors deliver pre-built, verified dual-core lockstep cores with integrated safety monitors, supporting ASIL D or B operations and the ISO 26262 automotive safety standard
- Security IP for cryptography and protocol acceleration offer platform security and secure boot
- Safety Manager IP Subsystem with FuSa SW stack to monitor, detect and report real-time random failures, and perform SoC level LBIST and periodic test

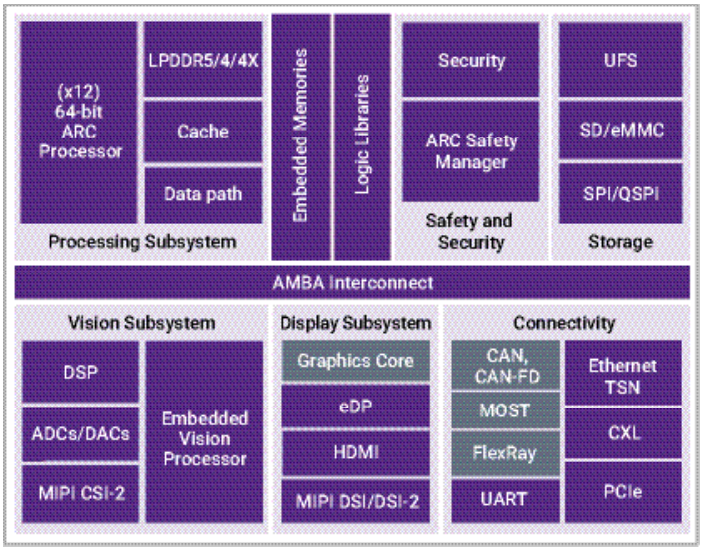

Figure 2: IP for ADAS SoCs

ISO 26262 Functional Safety

Safety-critical systems rely on SoCs and IP to meet Automotive Safety and Integrity Levels (ASILs) specific to each application. Synopsys' ASIL B and D compliant, automotive-grade IP portfolio is developed and assessed specifically for random hardware faults with ASIL D systematic. The ASIL B and D Ready, automotive-grade IP portfolio is developed and assessed specifically for random hardware faults. The DesignWare ARC EM22FS processor is compliant for both ASIL B or D random hardware faults and ASIL D systematic. Using certified IP helps SoC designers reduce supply chain risk and accelerate the requirements specification, design, implementation, integration, verification, validation and configuration of their SoC-level functional safety.

Benefits of Synopsys DesignWare IP for Functional Safety

- Synopsys "safety culture" implements policies, processes, strategies and safety managers (Semiconductor Automotive Functional Professional (SC-AFSP) certified) for safety-related IP development
- Enhanced safety features such as datapath protection, configuration register parity and ECC to memories
- IP delivered with ISO 26262 safety package
- Certified compliant by SGS-TUV Saar
- To see Synopsys' broad portfolio of ASIL Ready ISO 26262 certified DesignWare IP, visit synopsys.com

Connected Vehicle and Infotainment

Infotainment SoCs supporting real-time multimedia networks and incorporating the latest interface IP standards and protocols in emerging automotive operating systems require a broad, high-quality IP portfolio for automotive applications. Synopsys offers USB, LPDDR4, HDMI, MIPI, PCI Express®, mobile storage, security, data converters, logic libraries, embedded memories, Sensor and Control IP Subsystem, and ARC® Processors to speed connected vehicle and infotainment SoC development in the latest 28-nm and 16/14-nm FinFET process technologies. Synopsys also offers Ethernet IP that supports Time Sensitive Networking (TSN) standards and enables predictable and reliable networks for functional safety ADAS applications.

Benefits of Synopsys DesignWare IP for Connected Vehicle and Infotainment

- Multiple interfaces including LPDDR4, PCI Express, USB, DisplayPort, HDMI, MIPI, Ethernet AVB/TSN
- ARC EM, HS, and EV Functional Safety Processor IP supports ISO 26262 functional safety applications with integrated hardware safety features
- Security IP for HDCP 2.3 and DTCP-IP increases content protection

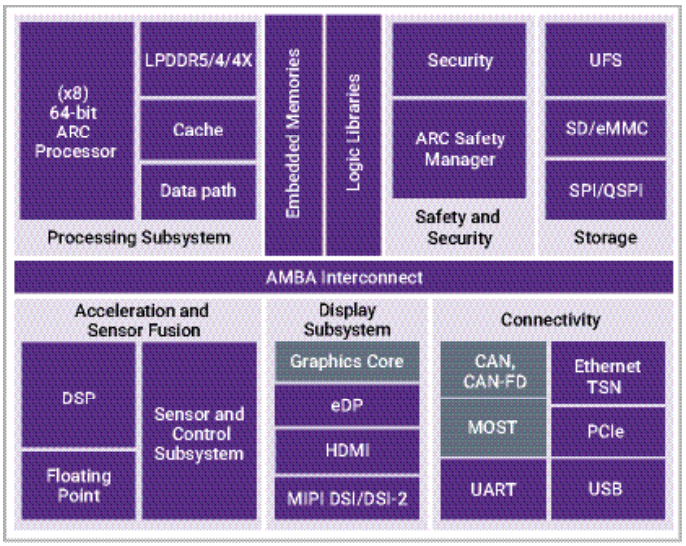

Figure 3: IP for connected vehicle and infotainment SoCs

Gateways

Gateway SoCs for automotive networks manage the system connectivity for domains applications. Synopsys offers a portfolio of silicon-proven IP including up to 10G Ethernet IP supporting time-sensitive networking (TSN) for real-time high-performance data connectivity, ARC processors with ASIL D safety capabilities for real-time data management, and security IP with root of trust for encryption/decryption and Root of Trust. With Synopsys' DesignWare IP, designers can accelerate the design of gateway SoCs used for advanced network processing and critical system management including secure Over-the-Air (OTA) software management.

Benefits of Synopsys DesignWare IP for Gateways

- Ethernet AVB/TSN IP enable data prioritization and data policy protocols
- ARC EM, HS, and EV Functional Safety Processor IP supports ISO 26262 functional safety applications with integrated hardware safety features
- Security IP provides key management, encryption/decryption, and root of trust

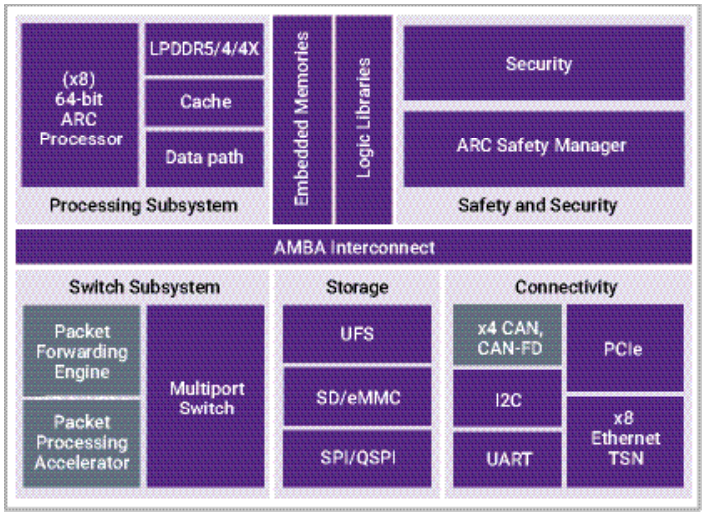

Figure 4: IP for gateway SoCs

Designed for Automotive Reliability

Synopsys DesignWare IP has been designed and tested in accordance to Synopsys' stringent automotive mission profile following automotive-specific design rules. Synopsys verifies our physical IP with very high-reliability automotive Parts Per Million (PPM) targets and critical specifications according to automotive Process Capability Index (Cpk) distributions.

Faster Time-to-Market

SoCs for ADAS, connected vehicles & infotainment and gateways are growing in complexity as they implement high-performance applications such as vision detection/correction as well as extensive multimedia content. To reduce the overall effort and cost of assembling and integrating IP into an SoC, Synopsys offers DesignWare IP Subsystems following an ISO 9001 quality and ISO 26262 functional safety process for ASIL readiness. The subsystems consist of pre-validated, fully integrated solutions that utilize Synopsys' automotive IP and tools for the specific SoC application. In addition, DesignWare IP Subsystems provide extra functionality and value over simply integrating a PHY and controller, e.g., common register interface between the PHY and controller, debug logic, and more. The Interface IP Subsystems include key protocols for automotive such as DDR, PCIe, USB, MIPI, and Ethernet, as well as multi-protocol subsystems.

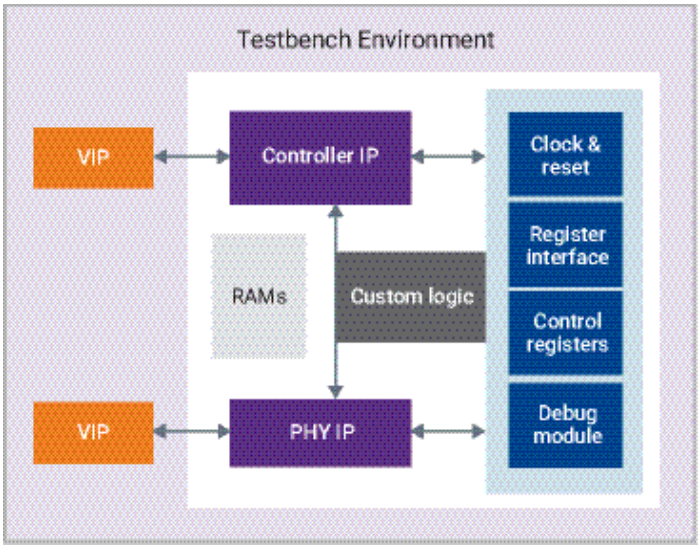

Figure 5a: DesignWare IP Subsystems

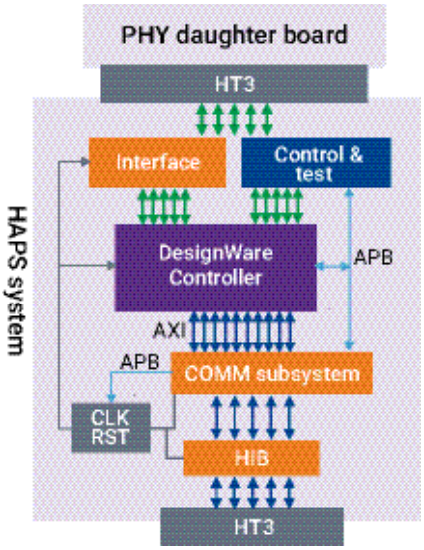

Figure 5b: DesignWare IP Prototyping Kits

DesignWare IP Prototyping Kits include a proven reference design of the target IP pre-tested on a HAPS FPGA-based prototyping system and software development platform running Linux OS. The pre-verified IP configuration can easily be modified to explore design tradeoffs for various automotive applications and offer a quick out of the box IP prototyping experience to accelerate software development.

DesignWare IP	Product Features for Automotive SoCs	Automotive ADAS SoCs Impact
Interface IP		
LPDDR5/4/4X Controller and PHY	Low latency, multi-port memory controller and PHY supporting LPDDR5/4/4X SDRAM speeds up to 6400 Mbps	Multi-port access to shared main memory enables protocol engines for embedded vision and high-performance heterogeneous processing
Ethernet AVB/TSN Controller	Ethernet supporting Audio Video Bridging, Time Sensitive Networking, and IEEE-1588 PTP with 1-step time stamping	Independent traffic classes and bounded latency enables precisely synchronized real-time camera and sensor data
MIPI CSI-2 and DSI/ DSI-2 Controllers, MIPI D-PHY, C-PHY/D-PHY	Integrated C-PHY/D-PHY IP supporting speeds up to 24 Gbps and MIPI CSI-2 and DSI/DSI-2 controllers	Enables multiple interoperable camera and display scenarios to support widest range of SoC applications
HDMI Controller and PHY	HDMI IP supporting the latest HDMI 2.1 with HDCP 2.3 specification	Ability to locate ADAS SoC remotely from video system
USB PHY	USB 2.0 and USB 3.0 PHYs are Temperature Grade 2 qualified. USB PHYs operate at USB 3.0/2.0 speeds, interoperable with all USB generations	Enables infotainment SoCs to support next-generation user interfaces with 4K and higher resolution video, imaging, audio and social media applications
PCI Express Controller and PHY	PCIe 3.0 & 4.0 with embedded DMA and debug features supporting endpoint, root port or dual mode operation; choose native or AMBA interfaces to support key automotive processors	Popular chip-to-chip interface to add processor peripherals. Low power L1 sub-states provide lowest power operation
Compute Express Link (CXL)	Supports data transfer speeds up to 32 GT/s and cache coherency for faster data access	Complex automotive systems with multiple CPUs and accelerators can maintain cache coherency between chips while moving data at high speeds
UFS Host Controller and PHY	Compliant with the latest JEDEC UFS, MIPI UniPro and MIPI M-PHY specifications, supports bandwidths up to 23.2 Gbps (2.9 GB/s) when high-speed Gear4 is used, and QoS features allow monitoring and training of the communication channel to enable a reliable link	Addresses the flash storage requirements of both ADAS and infotainment applications by enabling higher capacity, higher bandwidth and lower latency
Processor IP		
32-bit ARC Processor	ARC EM with Safety Enhancement Package (SEP) for ISO 26262 Functional Safety applications with integrated hardware safety features	Optimized for low-power embedded automotive applications, complete solution of processor IP; development tools and safety documentation accelerate development of ASIL D certifiable systems
EV Vision Processor	Lock-step safety island manages functional safety escalation for ADAS SoCs	Fast object detection and recognition for autonomous vehicles, ADAS applications, and in-camera driver detection
Foundation IP		
Embedded Memories	HPC Design Kit optimized for SoC processors: CPU, GPU and DSP; designed for demanding electro migration (EM) conditions; STAR Memory system with EEC support for multi-bit error correction	Enables optimal implementation across all three dimensions: performance, power, and area; SEU mitigation enables highest reliability
Embedded Test and Repair	STAR Memory System integrated test, repair and diagnostic solution for embedded memories. STAR Hierarchical System for automated hierarchical test for all IP and logic blocks on an SoC	Achieve low DPPM for designs needing up to ASIL D. Field algorithmic programmability and mission mode testing improve reliability for functional safety applications
NVM	AEC Q100 Temperature Grade 0 qualified NVM replaces eFuses for calibration and trimming applications; Synopsys portfolio includes multi-time programmable and one-time programmable NVM	Ideal for sensors, power management, LCD controllers, and precision analog
Analog IP		
12-bit SAR ADC	High resolution up to 12-bit, 320MSPS ADC/DAC converters; high dynamic range and high speed for extended application range; compatible with embedded flash	Integrated ADC reduces system form factor and extends application range for fast moving signal processing for multimedia and ADAS
Security IP		
Security IP	Broad array of content protection IP, hardware cryptographic engines and middleware, and embedded security modules with tRoot Secure Hardware Root of Trust for identification and authentication	Complete security IP portfolio helps prevent a wide range of evolving threats in connected cars such as theft, tampering, side channel attacks, malware and data breaches
IP Subsystem		
Sensor & Control IP Subsystem	Optimized to process data from digital and analog sensors. Offload host processors to enable more power-efficient processing of the sensor data; implemented using Synopsys' 32-bit ARC EM processor with ASIL D ISO 26262 Functional Safety Package	Reduces cost, complexity and development effort by pre-integrating sensor and actuator-specific IP blocks together with software in a single subsystem; enables sensor fusion by consolidating multiple sensor inputs to the SoC

For more information on DesignWare IP for automotive applications, visit synopsys.com/ip-automotive.

SYNOPSYS®
Silicon to Software™

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